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J.-S. Kim, A. M. Tyryshkin, and S. A. Lyon

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Annealing shallow Si/SiO₂ interface traps in electron-beam irradiated high-mobility metal-oxide-silicon transistors

J.-S. Kim,^{a)} A. M. Tyryshkin,^{b)} and S. A. Lyon^{c)}

Department of Electrical Engineering, Princeton University, Princeton, New Jersey 08544, USA

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Electron-beam (e-beam) lithography is commonly used in fabricating metal-oxide-silicon (MOS) quantum devices but creates defects at the Si/SiO₂ interface. Here, we show that a forming gas anneal is effective at removing shallow defects (≤ 4 meV below the conduction band edge) created by an e-beam exposure by measuring the density of shallow electron traps in two sets of high-mobility MOS field-effect transistors. One set was irradiated with an electron-beam (10 keV, 40 $\mu\text{C}/\text{cm}^2$) and was subsequently annealed in forming gas while the other set remained unexposed. Low temperature (335 mK) transport measurements indicate that the forming gas anneal recovers the e-beam exposed sample's peak mobility (14 000 cm^2/Vs) to within a factor of two of the unexposed sample's mobility (23 000 cm^2/Vs). Using electron spin resonance (ESR) to measure the density of shallow traps, we find that the two sets of devices are nearly identical, indicating the forming gas anneal is sufficient to anneal out shallow defects generated by the e-beam exposure. Fitting the two sets of devices' transport data to a percolation transition model, we extract a $T = 0$ percolation threshold density in quantitative agreement with our lowest temperature ESR-measured trap densities. *Published by AIP Publishing.* [<http://dx.doi.org/10.1063/1.4979035>]

Recent work on metal-oxide-silicon (MOS) quantum devices has demonstrated superb control of single electrons in electrostatically defined quantum dots.^{1–4} Silicon structures are a promising platform for the realization of a quantum processor,^{5,6} demonstrating long spin coherence times^{1,7,8} and a large valley splitting.^{8–10} In addition, silicon enjoys a mature fabrication infrastructure, thanks to the complementary MOS industry and is compatible with single ion implantation,^{11–13} allowing for electron-donor coupled qubits.^{13,14} One of the most pressing difficulties in fabricating MOS quantum devices is the presence of disorder at the Si/SiO₂ interface,⁸ specifically shallow defects a few meV below the conduction band edge (E_C). These shallow defects are of the same energy scale of a typical electrostatically defined quantum dot potential and are electrically active at the operating temperatures of a quantum dot device (< 1 K).^{1–3,8,15} In contrast, electrons confined in deeper, mid-gap states are frozen in place and are inert, contributing a static electric field background. As a result, the presence of shallow defects can be catastrophic for single electron control in quantum devices operating at low temperature. These interface traps can inadvertently be introduced during device fabrication by high energy processes, especially from e-beam lithography,¹⁶ the “workhorse” of quantum device fabrication in research labs.^{1–4,13,15,16} While a large body of literature exists on annealing irradiated Si/SiO₂ interface defects,^{17,18} most¹⁹ of these measurements are done well above liquid helium temperatures and characterize defects far away from the conduction band edge. Thus, little is known about annealing shallow traps which only manifest themselves at low temperatures.

We have fabricated devices with the highest reported electron mobility for a MOS field-effect transistor (MOSFET) with an oxide thickness of 30 nm or thinner^{8,20} (23 000 cm^2/Vs) and subjected these devices to e-beam irradiation and a subsequent forming gas anneal. Using electron spin resonance (ESR),^{21,22} we directly measure the shallow trap density of our devices and compare these results to more typical measurements of the Si/SiO₂ interface, namely, low temperature transport measurements of electron mobility^{8,16,20} and percolation thresholds.²³ Measurements of electron mobility are a commonly used method of assessing the oxide interface in MOS devices but provide only indirect measurements of confined shallow traps.²¹ Our transport data show that the e-beam dose significantly degrades a device's peak mobility, but a forming gas anneal can restore its peak mobility to within a factor of two of the unexposed sample's. Despite this difference in peak mobility, our devices display very similar $T = 0$ percolation threshold densities. Our ESR measurements of the density of shallow traps demonstrate that a forming gas anneal effectively removes shallow traps generated in the e-beam exposed sample over the entire measured energy range of approximately 4 meV (4.2 K) to 0.3 meV (360 mK) below the conduction band edge. We find our devices' lowest temperature ESR measurement of shallow traps match the $T = 0$ percolation threshold density, demonstrating agreement between two independent methods of assessing the oxide interface.

The devices measured in this work are n-channel inversion MOSFETs fabricated at Princeton from a commercially grown (Novati Technologies) gate stack. Our starting substrate consists of a high resistivity (1000–3000 $\Omega\text{-cm}$) float zone p-type (100) silicon wafer with 30 nm of dry, chlorinated thermal oxide and capped with 200 nm of un-doped amorphous silicon (a-Si). For both sets of devices, large-area MOSFETs ($3.3 \times 20 \text{ mm}^2$) were fabricated for ESR

^{a)}jk3@princeton.edu

^{b)}atyryshk@princeton.edu

^{c)}lyon@princeton.edu

measurements and Hall bars ($0.2 \times 4 \text{ mm}^2$) were fabricated for transport measurements. A large gate area ($\sim 1 \text{ cm}^2$) is necessary to detect the spin signal of 2D electrons at 4.2 K using X-band ESR.²² Holes were etched through the a-Si for self aligned ohmic contacts using an SF_6 and C_4F_8 based plasma and the underlying oxide was etched with buffered HF. The devices were implanted with As (35 keV, $5 \times 10^{15} \text{ cm}^{-2}$, Leonard Krock, Inc.) to dope the source/drain contacts as well as the a-Si gate. The n^+ a-Si was then etched in SF_6 and C_4F_8 to define the gate geometry. The samples were cleaned in an O_2 plasma for 10 min, RCA cleaned in quartz dishes, and annealed in N_2 (900 °C, 1 h) to activate the implanted dopants, crystallize the n^+ a-Si into poly-silicon, and to reduce fixed charge at the Si/SiO₂ interface.¹⁷

At this point, the process was split and one set of devices (samples B) received a blanket e-beam exposure (10 keV, $40 \mu\text{C}/\text{cm}^2$) and the other set (samples A) remained unexposed. The e-beamed samples were spin coated with 300 nm of ZEP520a e-beam resist prior to irradiation to ensure proper alignment of the exposure. The calculated penetration depth of 10 keV electrons through our resist and device stack is $\approx 1 \mu\text{m}$ (Casino²⁴), deep enough to damage the Si/SiO₂ interface. After stripping the e-beam resist, both sets of devices were metallized with 300 nm of thermally evaporated Al over the source/drain and n^+ poly-Si gate. Al was evaporated over the gate to avoid loading the ESR resonator by the resistive poly-silicon²⁵ and to accelerate the passivation of interface defects.²⁶ Thermal evaporations were chosen over e-beam evaporations in this process as the latter method creates X-rays that can further damage the Si/SiO₂ interface.¹⁶ Both sets of devices were then annealed in forming gas (5% H_2 , 435 °C) for 25 min. Finally, Ti/Au was thermally evaporated onto the contacts for soldering to the device. In addition to the two sets of devices mentioned above, a third Hall bar (sample C) was fabricated to demonstrate the damage created by the e-beam exposure. This sample was fabricated identically to sample A but was then coated with e-beam resist and received an e-beam exposure (identical to sample B) at the very end of processing, with no post-exposure anneal.

Transport measurements were done on all three sets of devices using standard low frequency lock-in techniques. Samples A and B were measured in a ³He cryostat (Janis Research) at temperatures between 335 mK and 4.5 K using a constant excitation current of 1.5 nA. The threshold voltage (V_{th}) of these two devices was measured to be $\approx 0.07 \text{ V}$ at 4.2 K and increases slightly with decreasing temperature to $\approx 0.2 \text{ V}$ at 335 mK. Sample C was measured at 4.2 K with an excitation current of 115 nA and its threshold voltage was measured to be 1.2 V, indicating approximately 10^{12} cm^{-2} net oxide charges (interface states and fixed oxide charge) created by the e-beam exposure. For each sample, electron densities (n) were calibrated by measuring the Hall resistivity in a 0.5 T field, and the mobility was extracted by standard four-terminal lock-in measurements of the sample resistivity. Mobility (μ) data are summarized in Figure 1 which shows a peak mobility for sample A of $23,000 \text{ cm}^2/\text{Vs}$ at $n = 6.3 \times 10^{11} \text{ cm}^{-2}$, $14,000 \text{ cm}^2/\text{Vs}$ at $n = 6.1 \times 10^{11} \text{ cm}^{-2}$ for sample B, and $<1,000 \text{ cm}^2/\text{Vs}$ at $n = 5.5 \times 10^{12} \text{ cm}^{-2}$ for sample C. Sample A demonstrates the highest reported electron mobility for a MOSFET with an oxide thickness of

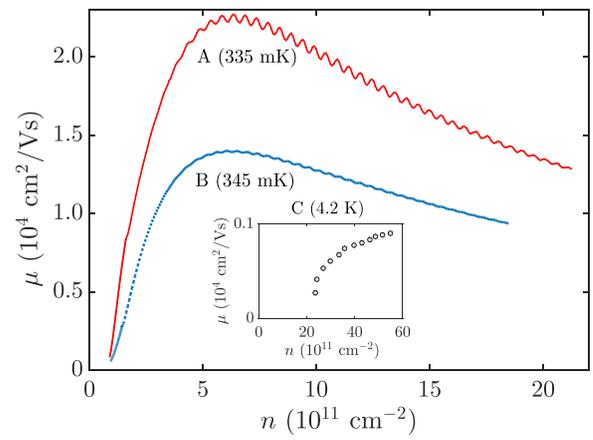


FIG. 1. Experimental mobility (μ) plotted as a function of electron density (n) for three studied devices. Sample A remained unexposed to the e-beam. Sample B was exposed and annealed in forming gas, recovering more than half of sample A's peak mobility. Sample C (inset) was exposed with no post-exposure anneal and shows significant degradation to its peak μ and a high threshold n . Shubnikov-de Haas oscillations are visible in samples A and B.

30 nm or thinner.^{8,20} Comparing the mobility data for all three devices show that the e-beam dose significantly degrades the oxide interface (sample C) and that a forming gas anneal is sufficient to restore an e-beamed device to high mobility (sample B).

Peak mobility, however, is measured at relatively high electron densities where the two dimensional electron gas (2DEG) can effectively screen out scattering centers²⁰ and as such is not necessarily a useful indicator of the oxide interface quality for quantum devices operating in the few electron regime.²¹ An alternative method used to assess the interface quality from transport measurements is to fit the measured conductivity (σ) to a percolation transition model²³ of the form $\sigma(n) = A(n - n_p)^p$ and extract the percolation threshold density (n_p). n_p gives a measure of the minimum number of carriers required to fill the disorder landscape before a conducting pathway can be supported. Holding the critical percolation exponent p at 1.31, the expected value for a 2D system,²³ and fixing the pre-factor A to the best-fit value obtained for each device at the lowest temperature measured, we extract a value of n_p at each measured temperature (Fig. 2). Using the functional form $n_p = n_0 + Ce^{-b/T}$, we can extrapolate the percolation threshold to zero temperature and extract n_0 , the $T = 0$ percolation threshold density.²³ The exponential term b is an energy gap related to the impurity distribution of the system. Our fit yields $n_p = 0.83 + 1.46e^{-2.25/T}$ for sample A and $n_p = 0.95 + 0.88e^{-3.00/T}$ for sample B, showing very similar $T = 0$ percolation thresholds of $0.83 \times 10^{11} \text{ cm}^{-2}$ and $0.95 \times 10^{11} \text{ cm}^{-2}$, respectively.

Using ESR, we can directly measure the density of electrons confined in shallow traps in samples A and B.^{21,22} We use X-band ($\sim 9.6 \text{ GHz}$, $\sim 3400 \text{ G}$) continuous wave ESR to measure the intensity of the 2DEG spin signal as a function of gate voltage (V_G) at fixed temperature between 360 mK and 4.2 K. Figure 3 shows an example of the number of unpaired spins, calculated as the double integral of the ESR spectrum, as a function of V_G . The data shown in Figure 3 are from sample B, measured at 1.50 K. As V_G is scanned

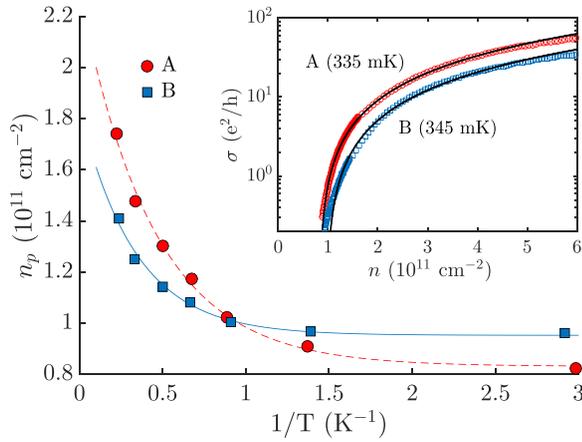


FIG. 2. Percolation threshold density (n_p) for samples A and B as a function of temperature. Fits to the form $n_p = n_0 + Ce^{-b/T}$ are also shown. Inset shows conductivity data (σ) vs. n and percolation fits with $p = 1.31$ to extract n_p for sample A at 335 mK and sample B at 345 mK.

below threshold, the ESR signal decreases as the shallow traps in the channel are thermally depopulated. At some V_G , the signal saturates (“dark” curve in Fig. 3) when the chemical potential is aligned with shallow traps deep enough that the confined electrons cannot thermally escape. We denote this characteristic voltage as V^* . Illuminating the sample with above band gap (1050 nm) light relaxes the system by neutralizing confined electrons with holes and the corresponding (“post-LED”) ESR signal decreases and eventually goes to zero at voltage V^0 .

With values for V^* and V^0 , we may then calculate the number of electrons confined in shallow traps (n_{conf}) at each measured temperature using the relation $e \cdot n_{conf} = C_{ox}(V^* - V^0)$, where C_{ox} is the oxide capacitance measured from the Hall resistivity. The energy scale of the shallowest populated traps at each temperature^{21,27} is approximately $10k_B \cdot T$. Figure 4 summarizes these data for samples A and B and plots data from a previous study for Ref. 21. We note that the samples studied in the current work demonstrate similar densities of shallow traps to the previously studied Sandia device.²¹ As temperature decreases, the

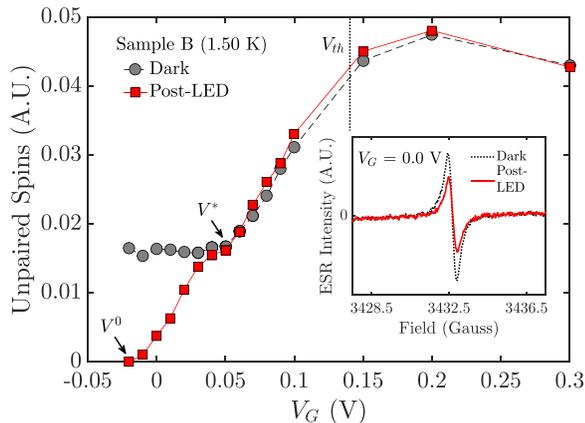


FIG. 3. Total number of unpaired spins plotted as a function of gate voltage for sample B at 1.50 K as measured in the dark (circles) and after above gap illumination (squares). $V_{th} = 0.14$ V at this temperature, shown by the dashed vertical line. Inset: ESR spectra at $V_G = 0.0$ V measured in the dark and after above gap illumination.

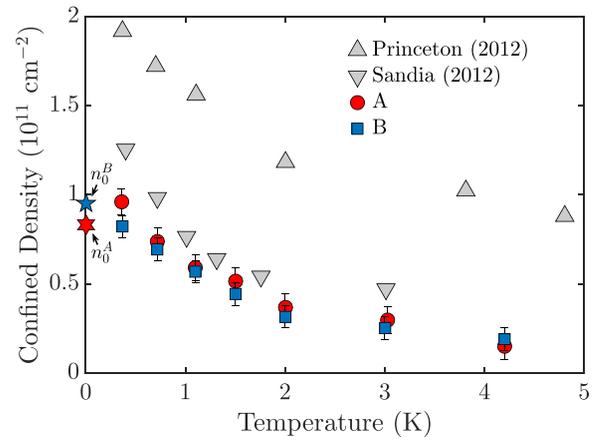


FIG. 4. ESR measurement of density of electrons confined in shallow traps as a function of temperature for samples A and B compared to previously studied devices (triangles). $T=0$ percolation threshold densities for A (hexagram) and B (pentagram) are also plotted on the axis. Data from the previously studied devices (“Princeton (2012)” and “Sandia (2012)”) were reproduced with permission from Appl. Phys. Lett. 100, 023503 (2012). Copyright 2012 AIP Publishing.

density of confined charge increases as more electrons are frozen into shallower traps. Within experimental error, samples A and B demonstrate the same density of shallow traps across the measured temperature range, $\approx 9 \times 10^{10} \text{ cm}^{-2}$ at ≥ 0.3 meV below E_C (360 mK) and $\approx 3 \times 10^{10} \text{ cm}^{-2}$ at ≥ 2 meV below E_C (2.0 K). This measurement is consistent with the $T=0$ percolation threshold densities for both devices studied ($n_0^{A,B}$), also plotted in Figure 4, and demonstrates the efficacy of the forming gas anneal for removing e-beam generated shallow defects across the measured energy range.

In summary, we have fabricated and measured high-mobility MOSFETs and have shown that a forming gas anneal is sufficient to restore an e-beam irradiated sample to the quality of an un-irradiated sample, as measured by the extraction of a $T=0$ percolation threshold and ESR measurements of the density of shallow traps. We believe that these measurements, as opposed to peak mobility, are more relevant metrics to characterize MOS interfaces for quantum devices operating in the low electron density regime and show that the two separate measurements agree with each other at the lowest measured temperature.

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