Double-Heterojunction Crystalline Silicon Solar Cell with Electron-Selective TiO$_2$ Cathode Contact Fabricated at 100ºC with Open-Circuit Voltage of 640 mV

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Abstract — A double-heterojunction c-Si solar cell was fabricated at maximum process temperature of 100ºC. We demonstrate an electron-selective passivated contact to Si using TiO$_2$, which increased the open-circuit voltage by 45 mV compared to a device with a direct metal to n-type substrate contact. In the fabricated structure, PEDOT/Si replaced the front-side p-n junction of conventional Si-based solar cells while the Si/TiO$_2$ interface is formed on the back-side. Compared to previous work [1], the $V_{OC}$ has increased from 620 to 640 mV while maintaining a maximum process temperature of 100ºC. Critical to the improved performance is better passivation of the Si/TiO$_2$ interface. The increase in $V_{OC}$ can be attributed to an interface recombination velocity of ~ 75 cm/s, which is consistent with photoconductance decay measurements.

Index Terms — carrier selective contact, heterojunction, passivation, metal-oxide, silicon, titanium oxide

I. INTRODUCTION

Recently there has been much interest in carrier selective contacts for crystalline silicon solar cells. Carrier selective contacts (CSCs) are a novel approach to realizing high-efficiency silicon solar cells without p-n junctions fabricated at high temperatures (> 800º). TiO$_2$ on Si(100) has been shown to blocks holes ($\Delta E_V \geq 2.3$ eV) while being transparent to electrons ($\Delta E_C < 0.3$eV) [2]. Furthermore, Si/TiO$_2$ interfaces have demonstrated effective minority carrier recombination velocities below 10 cm/s [3]. The combination of these properties makes TiO$_2$ an excellent choice for an electron-selective contact for high efficiency and low-cost Si-based photovoltaics.

Previously, we demonstrated a double-heterojunction crystalline silicon solar [1]. The front-side p+/n junction of a conventional Si solar cell was replaced by a heterojunction formed between n-Si and the organic polymer Poly(3,4-ethylenedioxythiophene) poly (styrenesulfonate) (PEDOT) that blocks electrons but passes holes [4]. The back-side n+/n junction was replaced by the electron-selective Si/TiO$_2$ heterojunction The band-alignment and structure is shown in Figure 1. We showed that the electron-selective TiO$_2$ contact increased $V_{OC}$ by 30 mV without degrading short circuit current or fill factor compared to a direct metal contact to the substrate. In this work, we show an increase of the effect of the TiO$_2$ contact on $V_{OC}$ from 30 mV to 45mV. We accomplished this through reducing interface recombination.

II. DEVICE PRINCIPLE

The effect of the TiO$_2$ is shown in Figure 2. A single-sided PEDOT/Si device (with no TiO$_2$) is displayed in Figure 2(a). The PEDOT/Si interface acts as a hole-selective contact, blocking electrons while being transparent to holes. Furthermore, due to the high work-function of the PEDOT, there is a depletion region in the silicon which collects photogenerated carriers. Because the electron dark current (majority carriers) is blocked by the PEDOT/Si interface, the dark current is now dominated by the hole dark current (minority carriers).

With the electron-selective TiO$_2$ deposited on the backside (Fig. 2(b)), the hole dark current is blocked. This leads to a further reduction in the dark current and thus an increase in the open-circuit voltage. However, in reality, the Si/TiO$_2$ interface will have defect states, allowing holes to recombine and thus negating the hole-blocking functionality of the Si/TiO$_2$ interface (Fig. 2(c)). The interface quality is typically described though an interface recombination velocity $S_{eff}$. We calculated $S_{eff}$ for different TiO$_2$ process conditions by measuring the minority carrier lifetime utilizing the Quasi-Steady State Photoconductance Decay (QSSPCD) method [5].

![Fig. 1. (a) Band-alignment at PEDOT/Si and Si/TiO$_2$ interface as measured by photoelectron spectroscopy. (b) Device structure [2]](image-url)
To elucidate the importance of interface recombination, one notes that the rate of hole transport in the substrate due to diffusion has to match the rate of recombination at the TiO$_2$ interface, which is proportional to the hole density at that interface. It is straightforward to show that the hole current ($J_{0,h}$) is reduced from its short base value $J_{0,SB}$ (no TiO$_2$) by a “blocking factor” BF, where

$$J_{0,h} = \frac{q n T D_p}{N_{D} W} * \frac{1}{BF} = J_{0,SB} * \frac{1}{BF}$$  \hspace{1cm} (1)$$

with \(BF = [(1+D_p/(W*S_{eff})] [1]. The calculated hole density profile is plotted in Figure 3 for an applied bias of 0.60V in dark (short-base scenario) for different $S_{eff}$ values. A lower $S_{eff}$ (smaller gradient) implies a higher BF and a smaller $J_0$. At $S_{eff} = 0$ cm/s, the gradient is completely flat. For an $S_{eff} > 10^3$ cm/s there is little effective blocking compared to a direct metal contact. Concomitantly, one can calculate an increase in $V_{OC}$ from the reduced $J_0$:

$$\Delta V_{OC} = kT * \ln \left( \frac{J_{0,no \ TiO_2}}{J_{0,TiO_2}} \right) = kT * \ln(BF) \hspace{1cm} (2)$$

Fig. 3. Simulated hole density profile for a 300 µm thick wafer for different $S_{eff}$ values. The applied bias is 0.60 V. Larger $S_{eff}$ values lead to larger gradients.

III. RESULTS AND DISCUSSION

To demonstrate the effect of the passivated TiO$_2$ contact, the two structures from Figure 2(a) and 2(b) - without and with TiO$_2$ respectively - were fabricated. Experimental details regarding fabrication are given elsewhere [1], with the exception that an additional step was performed: samples were left in N$_2$ ambient at room temperature for 48 hours. This step improved the passivation of the Si/TiO$_2$ interface to the same level as a 250°C anneal (measured by QSSPCD, before cathode deposition) [6]. J-V curves under light (solar simulator at ~ 110 mW/cm$^2$) are shown in Figure 4. The increase in $V_{OC}$ is consistent with the shift in dark current (inset). The relatively low $J_{SC}$ values are due to the lack of an effective AR coating, PEDOT absorption, and the cathode metal coverage. A slight increase in short-circuit current due to the TiO$_2$ can be attributed to increased collection of long wavelength photons as the Si/TiO2 interface is passivated and thus fewer photogenerated carriers recombine at the cathode.

Figure 5 shows the blocking factor as a function of $V_{OC}$ (from (2)) and $S_{eff}$ from the observed $V_{OC}$ (from (1)). Based on the experimentally observed increase in $V_{OC}$ of 45 mV, we find a BF of 5.4. Using $W = 300$ µm and assuming $D_p = 10$...
cm$^2$s$^{-1}$, we estimate $S_{\text{eff}}$ to be 75 cm/s. This $S_{\text{eff}}$ value is consistent with calculated $S_{\text{eff}}$ values from QSSPCD measurements of 65 - 85 cm/s at similar light levels.

Figure 6 shows a comparison between $S_{\text{eff}}(\Delta V_{\text{OC}})$, extracted from $\Delta V_{\text{OC}}$ using (1) and (2) and $S_{\text{eff}}(\text{PCD})$, determined from QSSPCD measurements of the TiO$_2$/Si interface left in N$_2$ ambient for 48 hours at room temperature (‘stabilized TiO$_2$’). Additionally, comparison between $S_{\text{eff}}(\Delta V_{\text{OC}})$ and $S_{\text{eff}}(\text{PCD})$ are made for $250^\circ$C annealed TiO$_2$ (‘annealed’ TiO$_2$’)) from previous experiments [6,7]. $250^\circ$C-annealed and room T-stabilized (this work) TiO$_2$ have similar $S_{\text{eff}}(\text{PCD})$ values. However $250^\circ$C-annealed TiO$_2$ has a large and high range for $S_{\text{eff}}(\Delta V_{\text{OC}})$. This indicates that although the $250^\circ$C annealing step reduces the recombination velocity measured by QSSPCD compared to as-deposited TiO$_2$, which typically has a $S_{\text{eff}}(\text{PCD})$ ~5000 cm/s, annealing at $250^\circ$C may lead to a morphology change (such as pinholes) which could allow the penetration of the cathode metal and thus increase $S_{\text{eff}}(\Delta V_{\text{OC}})$ and limits the effectiveness of $250^\circ$C annealed TiO$_2$ in a device.

**IV. CONCLUSIONS**

We have shown for the first time the use of an electron-selective TiO$_2$ contact to improve the open-circuit voltage of crystalline silicon solar cells by 45 mV to reach a $V_{\text{OC}}$ of 640 mV with a maximum process temperature of $100^\circ$C. The improvement in $V_{\text{OC}}$ can be attributed to a well-passivated Si/TiO$_2$ interface with a recombination velocity of 75 cm/s.

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